QSFPDD-400G-FR4

Optical SFP Module

400G QSFP-DD FR4 Transceiver, SM, 1310nm, 2KM

Features

- Supports 425Gb/s PAM4
- Built-in 400G PAM4 DSP
- Uncooled 4 channels 1310nm EML
- 4 channels PIN photo detector array
- Maximum link length of 2km SMF with KP-FEC
- Single MPO12 receptacle
- Hot pluggable QSFP-DD form factor
- Digital Diagnostics Monitoring Interface
- Commercial operating case temperature range: 0~ 70^{o} C
- Compatible with RoHS
- Power dissipation <10W
- TDECQ<3.4dB

Application

- 400G Ethernet
- Data Center
- Infiniband QDR
- Fiber channel

Standard

- IEEE 802.3bs 400GBASE-FR4
- QSFP-DD MSA compliant
- Compliant to SFF-8636

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Ambient Temperature	TSTG	-40	85	℃
Operating Humidity	HO	5	85	%
Power Supply Voltage	Vcc	-0.3	3.6	V
Signal Input Voltage		Vcc-0.3	Vcc +0.3	V

Recommended Operating Conditions

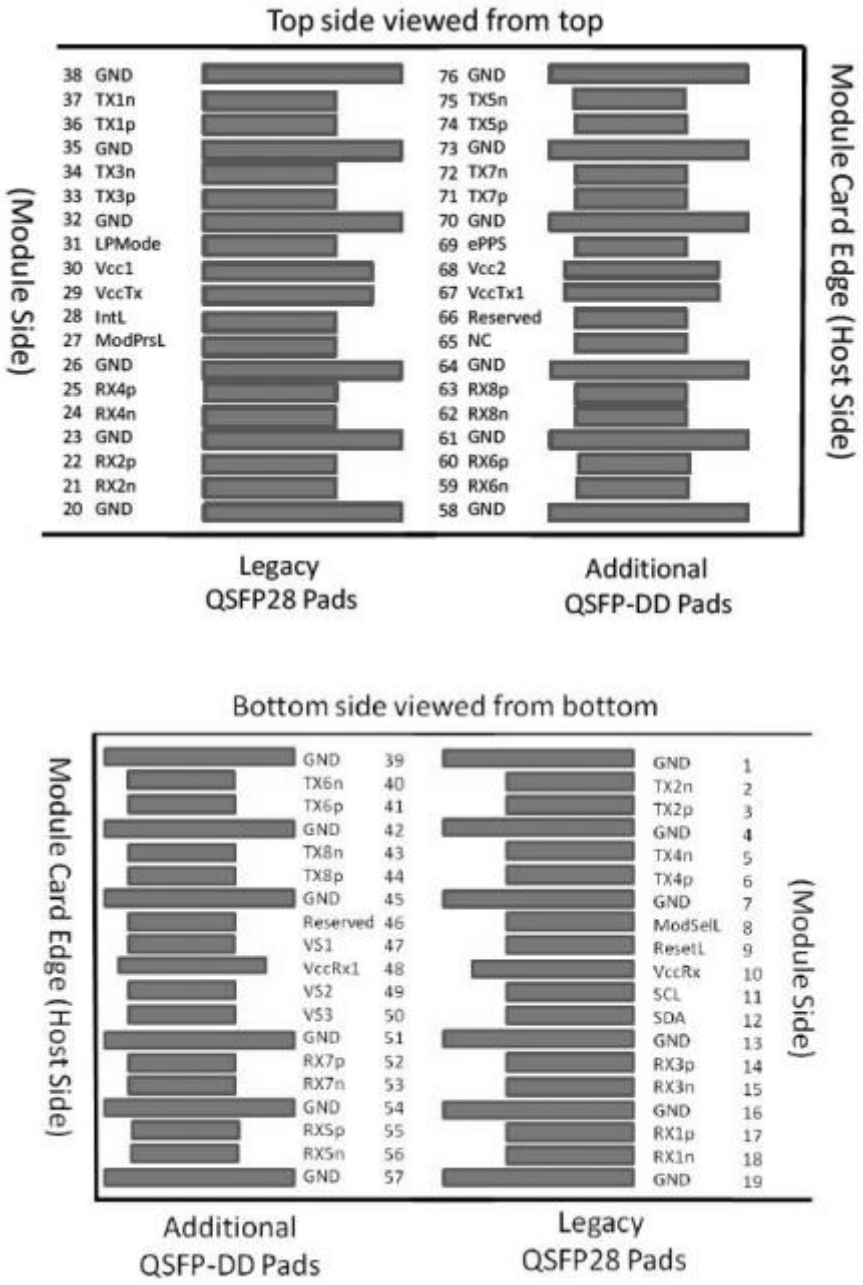
Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	℃
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Data Rate, each Lane (PAM4)			106.25		Gbps
Fiber Length 09/125μm core SMF		-	-	2	km

Optical and Electrical Characteristics

Optical Transmitter Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Launched Power (avg.) Per Lane	Pavg	-3.2		4.4	dBm	
Wavelength Range	λ0	1304.5	1310	1317.5	nm	
Spectral Width(-20dB)	∆λ			0.6	nm	
Extinction Ratio	ER	3			dB	
Transmitter OFF Output Power	POff			-30	dBm	
Optical Modulation Amplitude(OMA outer)	OMA	-1.46		3.7	dBm	
Transmitter and dispersion eye closure(TDECQ)	TDECQ			3.4	dB	
Optical Receiver Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Receiver Wavelength Range		1304.5		1317.5	nm	
Average Receiver Power Per Lane		-7.2		4.4	dBm	
Receiver Sensitivity Per Lane	Sen			-4.6	dBm	
Optical Power Input Overload	Pin-max	4.4			dBm	
Receiver Reflectance	Rr			-26	dB	

Pin Definitions

Pin Diagram



QSFP-DD MSA-compliant 76-pin connector

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	Ground	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	InitMode	Initialization mode; In legacy QSFP applica- tions, the InitMode pad is called LPMODE	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	

42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	Reserved	For Future Use	
47	VS1	Module Vendor Specific 1	
48	Vcc Rx1	+3.3V Power Supply Receiver	2
49	VS2	Module Vendor Specific 2	
50	VS3	Module Vendor Specific 3	
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	Ground	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output t	
64	GND	Ground	1
65	NC	For Future Use	
66	Reserved	Interrupt	
67	Vcc Tx1	+3.3V Power supply transmitter	2
68	Vcc2	+3.3V Power supply	2
69	Reserved	For Future Use	
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

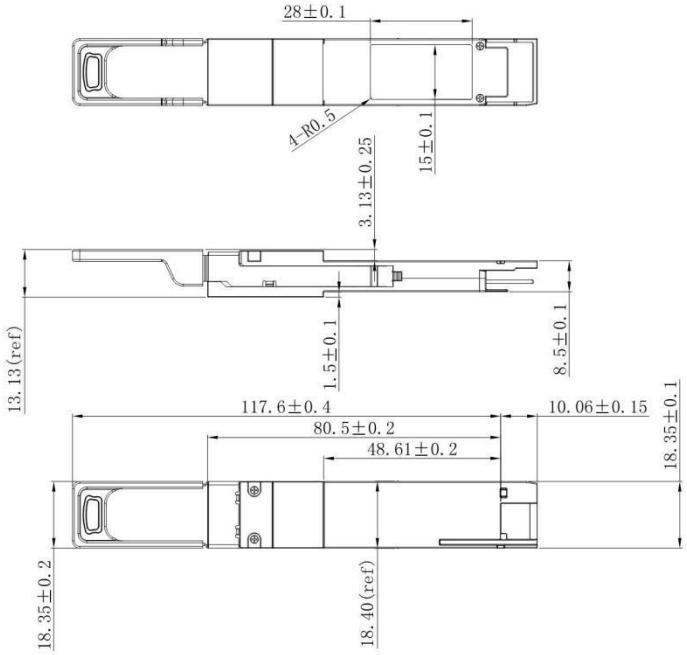
QSFP-DD Module PIN Definition

Notes：

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referred to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx andVccTx1 may be internally connected within the module in any combination. Each connector Vcc pin is rated for a maximum current of 1000 mA.

Mechanical Dimensions



Ordering information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (℃)	Reach (km)	DDM
QSFPDD-400G-FR4	QSFP-DD	400G	EML 1310	-3.2~4.4	PIN	<-4.6	0~70	2	Y

For further information, please visit our website https://www.aoatech.com